ABSTRACT

Method and apparatus for managing sensitive data. In one embodiment, sensitive data are managed in a circuit arrangement that includes a processor, a RAM, a register, a security circuit, and a power supply. The power supply is arranged to provide power from a first power source when power is available from the first source and from a second power source when power is unavailable from the first source. The processor initially stores the sensitive data in the RAM while operating with power from the first source. Upon loss of power from the first source, the power supply provides power from the second source, and the processor copies the sensitive data from the slow discharging RAM to the register and erases the sensitive data from the RAM. If the second power source is removed, the processor clears the sensitive data from the register. When the security circuit detects an attack on the circuit arrangement, the processor erases the sensitive data from the RAM and from the register.